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Attorneys for Plaintiff SYNOPSYS, INC. and for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC. and AEROFLEX COLORADO SPRINGS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, et al.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-2289 MJJ (EMC)

DECLARATION OF MICHAEL HEYNES IN SUPPORT OF DEFENDANTS' NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT OF NONINFRINGEMENT UNDER 35 U.S.C. §271(g)

Date: August 9, 2005
Time: 9:30 a.m.
Courtroom: 11, 19th Floor
Judge: Martin J. Jenkins

I, Michael Heynes, declare as follows:

1. I am a senior engineer with nearly forty years of experience developing and managing silicon chip fabrication technology. I was a principal contributor of technical content to the 2005 book "Demystifying Chipmaking." I have done consulting work and training on fabrication for numerous companies, including Applied Materials, Lam Research, Texas Instruments, and Motorola. I have been involved in the fabrication of at least one hundred different chips. I have a Ph.D. in Physical Chemistry from London University, where I wrote my thesis on Molecular Structure and Dielectric Properties of Silicates. I am a member of the Electrochemical Society and Institute of Electrical and Electronic Engineers (IEEE). My CV is attached hereto as Exhibit A. I make this Declaration of my personal knowledge, and if called as a witness, I could and would testify competently to the statements contained herein.

2. In forming the opinions set forth at the end of this declaration, I have considered and reviewed the text of United States Patent No. 4,922,432 ("the '432 patent").

3. ASIC design and chip manufacturing are separate phases. Very often these phases include separate companies, or at the very least, different departments within a company.

4. ASIC design culminates in the "tape out" of mask data. The mask data can then be used in photomask generation. The photomasks are subsequently used in ASIC manufacture. A chip is manufactured in layers; the overall layout is partitioned appropriately by the design software. Each layer is a pattern that must be reproduced on the wafer. These patterned layers, when stacked up, become the electronic components of the chip, all wired together. The individual layer patterns are transferred to the chip using a photolithographic technique. A template, called a photomask, is made for each layer.

5. Photomask manufacture includes the high level steps of:

i) photomask generation;
ii) prototype chip verification; and
iii) qualification for transfer to ASIC manufacturing.

6. Photomask generation includes many steps. These steps include, for each layer:

i) The mask-making company receives a computer file containing the design for each photomask.
ii) A blank, chrome-coated or other type of film-coated quartz glass plate is covered with photoresist or electron beam resist (photo-sensitive polymer or plastic sensitive to light or electron beams, respectively).
iii) Then the plate is processed in a computer-controlled electron beam (e-beam) tool or a laser pattern generator that exposes the desired pattern in the resist through multiple exposure steps. The mask data is used to produce the instructions for the machine that creates the pattern in the resist.
iv) Developer solution removes the unwanted resist, creating the desired pattern, and the pattern is inspected.
v) The remaining resist serves as the template (resist mask) for a wet etching process to remove the chrome not protected by the resist pattern.
vi) When the etching is completed, the resist mask is stripped off.
vii) The photomask receives a final inspection, and any defects are repaired.

7. The end result of the photomask generation steps is the creation of the desired pattern in the chrome or other layer on the glass surface, which can then be used as a mask. Typically, for state of the art chips, at least 25 to 30 masks are required to manufacture one chip design. Once the prototype photomasks have been finalized, the hundreds of steps necessary for actually manufacturing the integrated circuit can proceed using those photomasks.

8. After the prototype photomasks are generated, there is a prototype chip verification. This verification includes:

i) Running a small number of wafers using the new prototype photomasks;
ii) Electrically testing chips, in wafer form;
iii) Assembling and packaging chips; and
iv) Electrically testing packaged chips.

9. Once prototype chip verification is complete, the qualification for transfer to ASIC manufacturing occurs. Qualification includes up to thousands of computer-controlled electrical tests to characterize the product in terms of performance. Qualification can also include reliability testing, such as burn-in and temperature/humidity tests.

10. After the prototype chip verification and qualification are successfully completed, the photomasks are considered to be finalized.

11. The high level steps of ASIC manufacture include:

i) wafer fabrication; and
ii) assembly and test.

12. ASIC manufacture begins with wafer fabrication. Typically, many hundreds of ASIC chips are formed on a single wafer. Wafer fabrication minimally involves many hundreds of individual steps. These steps can be broken down and fall into two categories, the front end of the line (FEOL) and the back end of the line (BEOL). In the FEOL, the transistors and other devices are formed in and on the wafer surface. In the BEOL, the devices are wired together with metallization processes and the circuit is protected with a final sealing layer. These manufacturing steps typically include, but are not limited to, processes such as chemical vapor deposition, physical vapor deposition, etching, and chemical mechanical polishing.

13. After wafer fabrication, the circuits on the wafer are complete, but still in wafer form and have not yet been tested. During wafer sort, each chip is electrically tested for functionality. Once the functional chips are identified, packaging begins. The industry also refers to this phase of chip manufacture as assembly and test (A/T). During this phase, the wafers are separated, or diced, into individual chips, and the functional chips are placed into protective packages. Packaging typically takes place in a separate department of the semiconductor producer or often in a foreign plant. After packaging, there are further electrical tests, which are even more extensive than the electrical tests carried out at the wafer level.

14. The wafer fabrication processes fall into four basic operations. They are layering, patterning, doping, and heat treatments. These processes are used repeatedly in the wafer fabrication process. The exact sequence is determined by the "construction" of the transistor used along with other physical attributes of the circuit components, and the interconnection wiring of the circuits.

i) Layering (otherwise known as thin film formation): Layers used in the circuit as dielectrics, conductors, or semiconductors are grown or deposited on the wafer surface. Ways of forming layers or films include chemical vapor deposition, physical vapor deposition, and oxidation.

ii) Patterning: The electrical functioning of an IC is dependent on the physical dimensions of the components formed in and on the wafer surface and the electrical characteristics (such as electrical carrier concentrations, and the electrical resistance at the wafer surface). The vertical dimensions (d) are created by the thickness of the layers and by the depth of the doped regions.

The horizontal dimensions (w and l) are created during the patterning process. This process uses a mask, as described above, which has the required horizontal dimensions and the relative position of the components set in chrome on a glass

plate. The mask is used as a stencil to transfer the mask dimensions into a layer of a photoresist. The resultant image in the photoresist is generally transferred into the wafer surface through an etching process.

The steps in patterning include:
1. Baking wafers and priming surfaces.
2. Coating wafers with photoresist, known as spinning.
3. Softbaking to evaporate solvents.
4. Aligning and exposing pattern in photoresist.
5. Developing resist to remove exposed photoresist.
6. Hardbaking to harden the photoresist.
7. Inspecting for defects, contamination, measuring pattern dimensions, pattern distortions, etc.
8. Etching to remove unwanted material through openings in the photoresist.
9. Removing photoresist.
10. Final inspection for defects, contamination, measure pattern dimensions, pattern distortions, etc.

iii) Doping: Electrically active chemical elements are put into the wafer surface to modify the electrical properties of the silicon through ion implantation or diffusion techniques.

iv) Heat Treatments: Many thermal processes are involved throughout the wafer fabrication cycle for many different purposes, such as low temperature steps to evaporate solvents from the photoresist, and high temperature steps to grow thin oxide films on the silicon.

15. The conclusion of the wafer fabrication process is the wafer sort to identify the functioning chips.

16. After the wafers are fabricated and sorted, assembly and test occurs. Assembly and test includes several steps, including:

i) Wafer Backside Preparation: To thin the wafer in preparation for packaging.
ii) Die Separation: To cut individual chips from the wafer.
iii) Die Pick: To select functioning die and place them in package.
iv) Die Attach: To attach the die to the package.
v) Wire Bonding: To connect leads between die and package.
vi) Pre Seal Inspection: To inspect wire bonding.
vii) Seal: To encapsulate the die in the package.
viii) Marking: To identify product.
ix) Final Electrical and Environmental Tests: To test that chips fully meet customer specifications.

17. After the chips finish the assembly and test process, they are packed and shipped to the customer.

18. Based on claims 13-17 and the '432 patent's description, it is my opinion that claim 13-17's processes are not directed to manufacture at all, rather they are completely directed toward design. Therefore, Claim 13-17's processes are not processes for "directly manufacturing" ASIC chips.

19. While the design information, particularly the mask data, is used in the manufacture of photomasks, it is not used directly in the manufacture of ASIC chips. None of these steps following the "tape out" is part of the patented process of the '432 Patent.

20. As described above, the mask data is subsequently used in other processes to produce masks, not ASIC chips. The claimed processes for generating netlists and mask data are not even steps in the manufacture of masks, let alone ASIC chips. There are many manufacturing steps that lie between the end product of the processes of the '432 patent and masks, and many hundreds of additional manufacturing steps that lie between the masks and the manufactured ASIC chips.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration was executed in San Mateo, California on June 14, 2005.

Dr. Michael Heynes

EXHIBIT A

Michael S. Heynes

1501 W. Hillsdale Blvd., #111, San Mateo, CA 94402
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Overview

Senior engineer with broad semiconductor industry experience managing silicon chip fabrication technology, primarily in CMOS.
Managed engineering groups responsible for new product and new process module development, in both MOS and bipolar technologies.
Managed technology transfer and bring-up of new manufacturing equipment and facilities.
Much work in training in recent years.

Work Experience

Consultant **7/98 to date**

Primarily engaged in technical training

- Generated and taught classes on a wide range of semiconductor industry topics.
- Wrote and reviewed scripts for training videos.
  Reviewed and advised on drafts for technical publications and product marketing brochures (in association with Semiconductor Services).

Lam Research Corp., Fremont, CA **95 –98**

Senior instructor
Developed and presented classes on a range of semiconductor topics with emphasis on applications of Lam equipment in chip manufacturing.

Teledyne Components, Mountain View, CA **90-95**

Senior Staff Scientist
Developed and transferred to manufacturing CMOS and bipolar process technology for digital and analog circuit applications.
Carried out a study to evaluate difficulties and market potential for micro-machined sensors (MEMS)

Previous positions

- Senior Member Technical Staff, Gain Electronics (Somerville, NJ)
  A Bell Laboratories spin-off formed to produce digital gallium arsenide chips.
- Manager, CMOS Technology Development, American Microsystems
  (Santa Clara and Pocatello, Idaho)
  Included two year assignment to acquire and bring up new equipment and transfer CMOS manufacturing technology to a new joint-venture operation with a major company in Austria.

- Manager, IC Pilot Line, Microtechnology, (A Sunnyvale CMOS start-up, later acquired by Storage Technology.)
  Responsible for running new chip design prototypes.
- Director, Process Technology Development, Nortec Electronics, an early MOS start-up in Santa Clara.
  Developed a range of MOS technology processes.

- Early work at Signetics(Philips), Raytheon, Shockley Transistor included silicon crystal and epitaxial film growth, chemical vapor deposition (CVD), oxidation, diffusion, development of bipolar RF/ microwave power transistors.

Education
B.Sc., Chemistry, Birmingham University, England
Ph.D., Physical Chemistry, London University, England
(Molecular Structure and Dielectric Properties of Silicates)

Principal contributor of technical content to book : "Demystifying Chipmaking" Yanda, Heynes, Miller. (Elsevier 2005; ISBN 0-7506-7760-0)

Member, Electrochemical Society and IEEE (Institute of Electrical and Electronic Engineers)